a first interlayer insulating film over said insulating film;

a second interlayer insulating film on said first interlayer insulating film, said second interlayer insulating film comprising a different material from said insulating film;

a first opening in said insulating film for exposing a portion of said semiconductor layer;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor layer and a portion of said insulating film where surrounds said first opening; and

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor layer, said portion of said insulating film and a portion of said first interlayer insulating film where surrounds said second opening,

wherein edges of at least said third opening are rounded off.

C1 cont.

2. (Amended) A device according to claim 1 wherein a taper angle β of the second interlayer insulating film with respect to a major surface of said semiconductor layer in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to the major surface of said semiconductor ~~layer in the second opening~~

6. (Amended) A semiconductor device comprising:

a semiconductor layer formed over a substrate having an insulating surface, said semiconductor layer having at least channel, source and drain regions;

a gate insulating film over said semiconductor layer;

a first interlayer insulating film over said gate insulating layer;

a second interlayer insulating film on said first interlayer insulating film, said second interlayer insulating film comprising a different material from said gate insulating film;

a first opening in said gate insulating film for exposing a portion of said semiconductor layer;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor layer and a portion of said gate insulating film where surrounds said first opening; and

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor layer, said portion of said gate insulating film and a portion of said first interlayer insulating film where surrounds said second opening,

wherein edges of at least said third opening are rounded off, and

wherein a taper angle β of the second interlayer insulating film with respect to a major surface of said semiconductor layer in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to the major surface of said semiconductor layer in the second opening.

~~10. (Amended)~~ A semiconductor device comprising:

a semiconductor layer having at least channel, source and drain regions;

an insulating film on said semiconductor layer

a first interlayer insulating film over said insulating film;

a second interlayer insulating film on said first interlayer insulating film;

a first opening in said insulating film for exposing a portion of said semiconductor layer;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor layer and a portion of said insulating film where surrounds said first opening;

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor layer, said portion of said insulating film and a portion of said first

interlayer insulating film where surrounds said second opening; and

an electrode formed on said first, second, and third openings and connected with one of said source and drain regions through said first, second, and third openings,

wherein a taper angle β of the second interlayer insulating film with respect to a major surface of said semiconductor layer in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to a major surface of ~~said semiconductor layer in the second opening.~~

11. (Amended) A device according to claim 10, wherein said insulating film comprises silicon oxide.

~~14. (Amended) A semiconductor device comprising:~~

a semiconductor layer including at least channel, source and drain regions;

an insulating film on said semiconductor layer

multi-interlayer insulating films comprising at least an upper insulating layer and a lower insulating layer over said insulating film, said lower insulating layer comprising the same material as said upper insulating layer; [and]

at least one contact hole in said multi-interlayer insulating films and said insulating film, said contact hole having a tapered section; and

an electrode formed on said contact hole and connected with one of said source and drain regions through said contact hole,

wherein a taper angle β of an inner surface of the upper insulating layer in the contact hole with respect to a major surface of said semiconductor layer is larger than a taper angle α of an inner surface of the lower insulating layer in the contact hole with respect to said major surface of said ~~semiconductor layer~~.

16. (Amended) A device according to claim 14, wherein said lower and upper insulating layers comprise a material selected from the group consisting of silicon nitride and organic resin.

~~19.~~ (Amended) A semiconductor device comprising:

a semiconductor layer having a channel region, at least one low doped impurity region, and at least one high doped impurity region said high doped impurity region being adjacent to said channel region with said low doped impurity region interposed therebetween;

an insulating film on said semiconductor layer;

an interlayer insulating film comprising a plurality of insulating layers over said semiconductor layer and said insulating film; and

a contact hole in said interlayer insulating film and said insulating film for exposing a portion of said high doped impurity region, said contact hole has a tapered section,

wherein edges of said interlayer insulating film in said contact hole are rounded off, and

wherein angles of the tapered section of the contact hole decrease successively from a top interlayer insulating layer ~~toward a bottom interlayer insulating layer.~~

~~24.~~ (Amended) A semiconductor device comprising:

a semiconductor layer having a channel region, at least one low doped impurity region, and at least one high doped impurity region said high doped impurity region being adjacent to said channel region with said low doped impurity region interposed therebetween;

an insulating film on said semiconductor layer;

an interlayer insulating film comprising a plurality of insulating layers over said semiconductor layer and said insulating film; and

a contact hole in said interlayer insulating film and said insulating film for exposing a portion of said high doped impurity region, said contact hole has a tapered section; and

an electrode formed on said contact hole and connected with one of said source and drain regions through said contact hole,

wherein edges of said interlayer insulating film in said ~~contact hole are rounded off.~~

Please add new claims 31-37.

--31. (New) A device according to claim 1, wherein edges of said first opening are rounded off.

32. (New) A device according to claim 1, further comprising an electrode connected with one of said source and drain regions through said first, second, and third openings.

33. (New) A device according to claim 6, wherein edges of said first opening are rounded off.

34. (New) A device according to claim 6, further comprising an electrode connected with one of said source and drain regions through said first, second, and third openings.